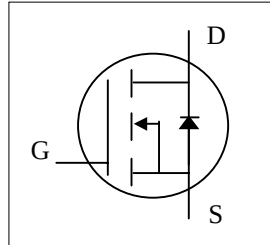
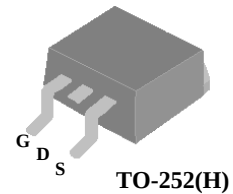




- ▼ 100% R_g & UIS Test
- ▼ Fast Switching Characteristic
- ▼ Simple Drive Requirement
- ▼ RoHS Compliant & Halogen-Free



BV_{DSS}	650V
$R_{DS(ON)}$	$0.38\ \Omega$
I_D^3	10A



Description

AP65SL380D series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-252 package is widely preferred for commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

Absolute Maximum Ratings@ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	650	V
V_{GS}	Gate-Source Voltage	± 20	V
V_{GS}	Gate-Source Voltage, AC ($f > 1\text{Hz}$)	± 30	V
$I_D@T_C=25^\circ\text{C}$	Drain Current, V_{GS} @ $10V^3$	10	A
$I_D@T_C=100^\circ\text{C}$	Drain Current, V_{GS} @ $10V^3$	6.5	A
I_{DM}	Pulsed Drain Current ¹	24	A
dv/dt	MOSFET dv/dt Ruggedness ($V_{DS} = 0 \dots 400V$)	40	V/ns
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation	78.1	W
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation ⁶	2	W
E_{AS}	Single Pulse Avalanche Energy ⁴	75	mJ
dv/dt	Peak Diode Recovery dv/dt^5	15	V/ns
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Units
R_{thj-c}	Maximum Thermal Resistance, Junction-case	1.6	$^\circ\text{C}/\text{W}$
R_{thj-a}	Maximum Thermal Resistance, Junction-ambient (PCB mount) ⁶	62.5	$^\circ\text{C}/\text{W}$



AP65SL380DH

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	650	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =3.2A	-	-	0.38	Ω
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	2	-	5	V
g _{fs}	Forward Transconductance	V _{DS} =15V, I _D =3.2A	-	6	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =520V, V _{GS} =0V	-	-	100	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±1	uA
Q _g	Total Gate Charge	I _D =5A	-	33	52.8	nC
Q _{gs}	Gate-Source Charge	V _{DS} =480V	-	8	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =10V	-	14	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DD} =300V	-	13	-	ns
t _r	Rise Time	I _D =5A	-	11	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω	-	33	-	ns
t _f	Fall Time	V _{GS} =10V	-	8	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	1160	1860	pF
C _{oss}	Output Capacitance	V _{DS} =100V	-	40	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	5	-	pF
R _g	Gate Resistance	f=1.0MHz	-	3.3	6.6	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =3.2A, V _{GS} =0V	-	0.8	-	V
t _{rr}	Reverse Recovery Time	I _S =5A, V _{GS} =0V	-	120	-	ns
Q _{rr}	Reverse Recovery Charge	di/dt=100A/μs	-	710	-	nC

Notes:

- 1.Pulse width limited by max. junction temperature.
- 2.Pulse test
- 3.Limited by max. junction temperature. Maximum duty cycle D=0.75
- 4.Starting T_j=25°C , V_{DD}=50V , L=150mH , R_G=25Ω
- 5.I_{SD} ≤ I_D, V_{DD} ≤ BV_{DSS}, starting T_j = 25°C
- 6.Surface mounted on 1 in² copper pad of FR4 board

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

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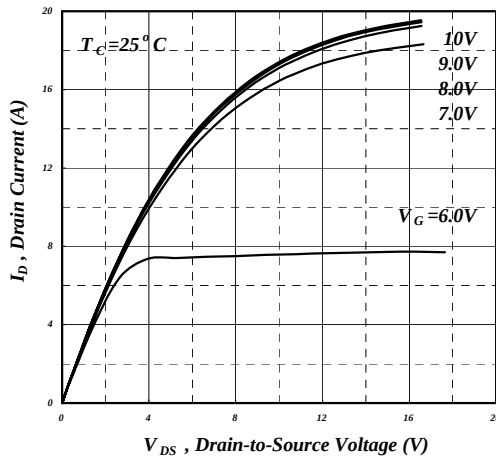


Fig 1. Typical Output Characteristics

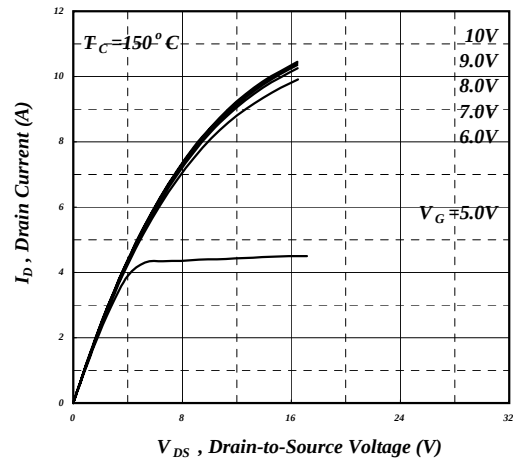


Fig 2. Typical Output Characteristics

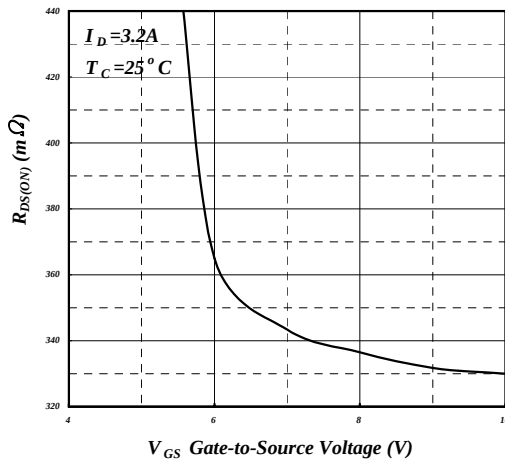


Fig 3. On-Resistance v.s. Gate Voltage

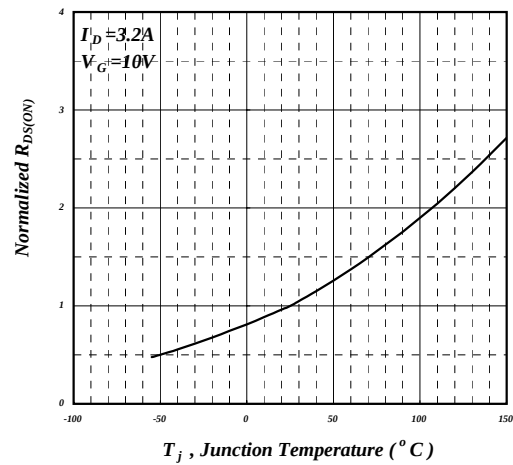


Fig 4. Normalized On-Resistance v.s. Junction Temperature

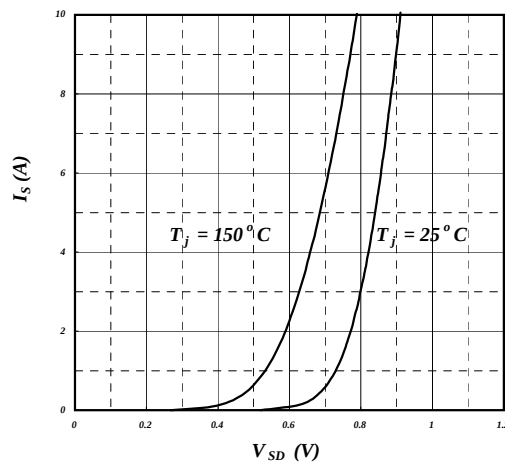


Fig 5. Forward Characteristic of Reverse Diode

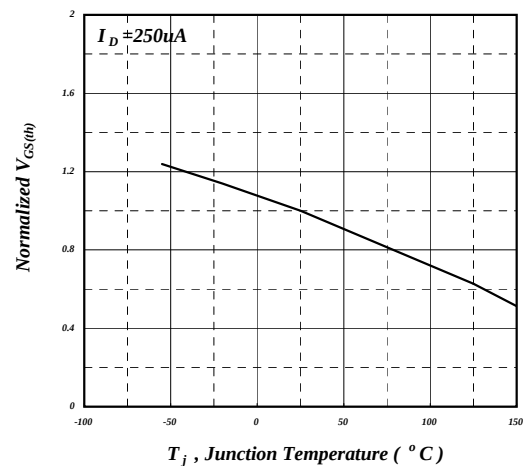


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

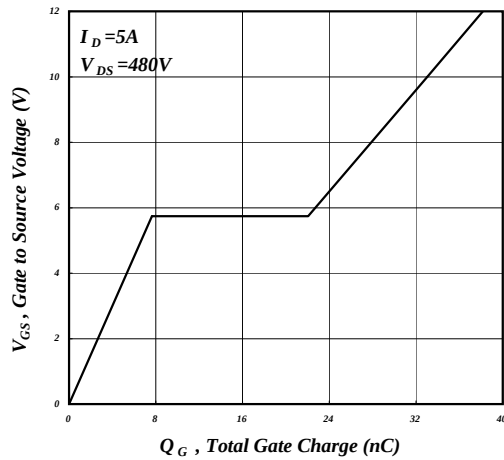


Fig 7. Gate Charge Characteristics

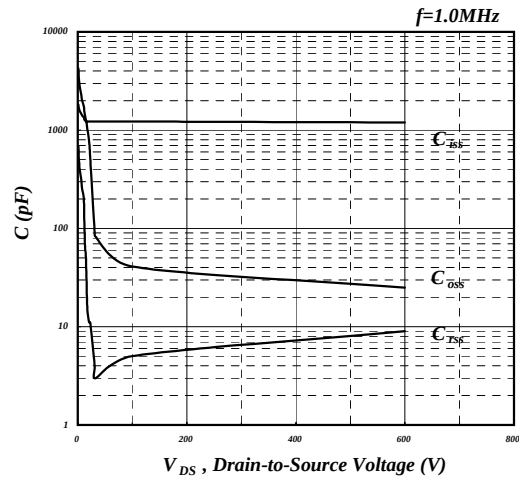


Fig 8. Typical Capacitance Characteristics

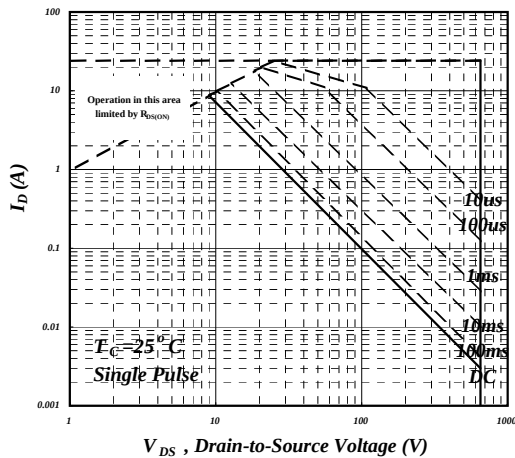


Fig 9. Maximum Safe Operating Area

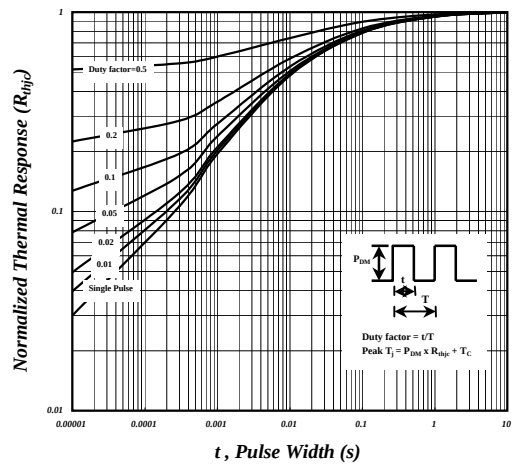


Fig 10. Effective Transient Thermal Impedance

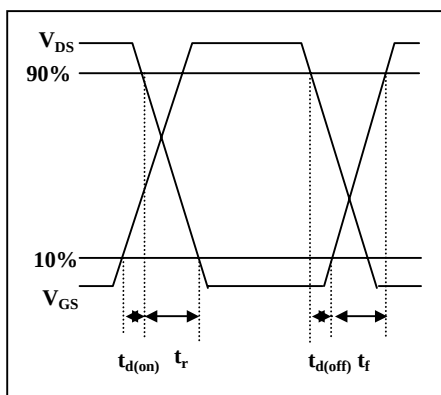


Fig 11. Switching Time Waveform

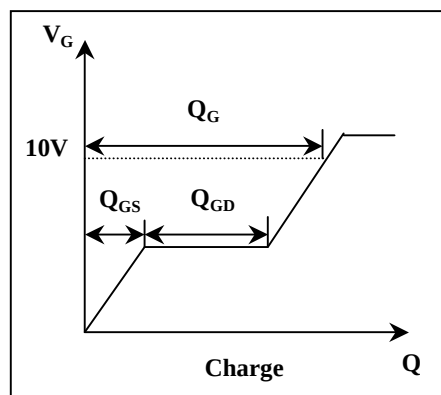


Fig 12. Gate Charge Waveform

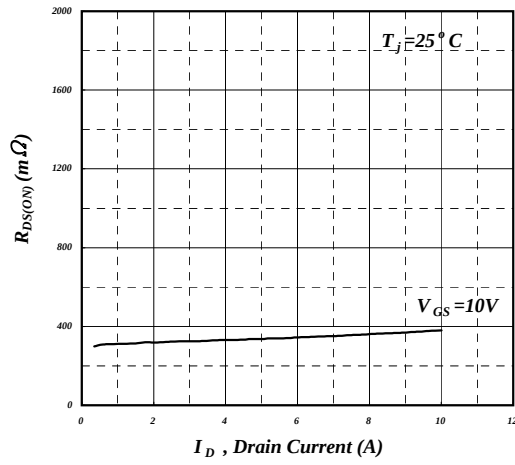


Fig 13. Typ. Drain-Source on State Resistance

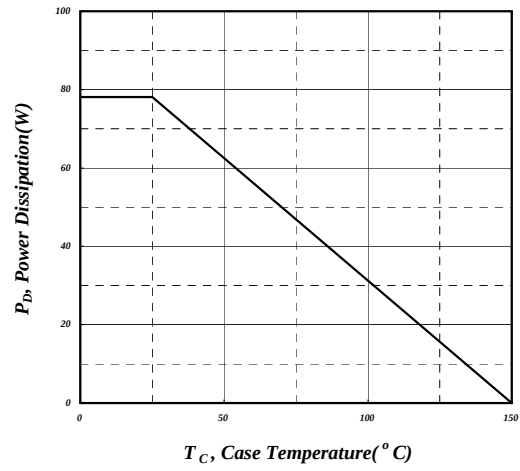


Fig 14. Total Power Dissipation



AP65SL380DH

MARKING INFORMATION

